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 25. A substrate-based packaged electronic device as in Claim 1, wherein the degating region extends to an edge of the package encapsulant.--

REMARKS

The paragraphs below are numbered below to correspond with the paragraph numbering used by the Examiner in the Office Action.

1/2/3/4. Restriction requirement under 35 U.S.C. § 121.

Claims 1-14 and new Claims 23-25 remain in this application. Claims 15-22 have been canceled. Applicants hereby affirm the election of Claims 1-14 drawn to the substrate-based packaged electronic device made by Applicants' Attorney on 3/15/96.

5. Rejection of Claims 13 and 14 under 35 U.S.C. § 112, fourth paragraph.

The Examiner rejected Claims 13 and 14 as being of improper dependent from for failing to further limit the subject matter of a previous claim. In response to the Examiner's rejection, Claim 13 has been amended to depend on, and further limit, Claim 11. Claim 14 depends on, and further limits, Claim 13.

As a result, Claims 13 and 14 meet the requirements of 35 U.S.C. § 112, fourth paragraph and it is requested that this rejection be withdrawn.

6/7. Rejection of Claims 1-9 and 11-14 under 35 U.S.C. § 103 as being unpatentable over Mullen, III et al. in view of Erdos.

The Examiner states:

Mullen does not disclose: a degating region or the material gold of which it is comprised of; a mold runner; or the relative adhesive limits of the encapsulant material, degating region, or the substrate material.

Erdos discloses an encapsulated IC chip package formed by degating (see abstract) whereby the package has a degating region - carrier tape 10 made of metal (col. 4, lines 53-54) and a mold runner - runner components (col.

LAW OFFICES OF
 SKIERNEN, MORRILL,
 McPHERSON, FRANKLIN
 & FRIEL

25 METRO DRIVE
 SUITE 700
 SAN JOSE, CA 95110
 (408) 453-9200
 FAX (408) 453-7979

5, lines 60-61).

The Examiner is correct that Mullen, III et al. does not disclose a degating region, a mold runner or the relative adhesive limits of the encapsulant material, degating region, or the substrate material. Thus, Mullen, III et al. does not teach or suggest "a degating region on the first surface of the substrate" and "a degating region material on the degating region", as recited in Claim 1, as amended. Applicants were well aware of Mullen, III et al. because Bruce J. Freyman was a co-inventor thereof.

In regards to Erdos, the Examiner's statement is respectfully traversed. In reference to Erdos Figs. 1 and 2:

a metal coated plastic tape carrier 10 carrying integrated circuit chips 12 is shown. The chips 12 are centered in apertures 16 formed in the tape carrier 10, ready for encapsulation. (Col. 3, lines 45-54.)

The mold opening procedure, after encapsulation, is described in reference to Figs. 13, 14, 15, 10 (Column 5, line 48 to Column 6, line 32). In particular:

Initially, as shown in Fig. 13, the mold halves 34, 40, including lower cavity part 36 and slide 38, are all closed about the carrier tape 10 and encapsulated chips 12a. Then, firstly the upper mold half 40 is raised ... As the upper mold half 40 is raised, the ejector pins 70 in the lower cavity part half 36 at the same time follow the upper mold half 40 upwardly, retaining the encapsulated chips 12a securely in the upper mold cavity halves 54 and thereby breaking (degating) the encapsulated chips from the plastic in the runner system. Since the plastic in the runner system is connected to the encapsulated chips only by the plastic in the very small gate openings 116 formed by the space between lower end walls 62a and mold surface 52, little force is applied to the encapsulated chips 12a during this chip ejection procedure. (col. 5, lines 51-66, emphasis added.)

Thus, auto degating is achieved since the part is ejected while pinning the hardened plastic in the runner system in place (by the slide 38). (col. 6, lines 54). The plastic encapsulant never contacts the tape carrier during the fabrication process (col. 5, lines 39, 40, and col. 6, lines 45, 46, emphasis added).

Thus, Mullen, III et al. in view of Erdos does not teach or suggest "a degating region on the first surface of the

LAW OFFICES OF
SKJRVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

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substrate" and "a degating region material on the degating region", as recited in Claim 1, as amended.

Further, since Mullen, III et al. in view of Erdos does not teach or suggest "a degating region" as recited in Claim 1, as amended, Mullen, III et al. in view of Erdos does not teach or suggest "the degating region being formed outside the package encapsulant" and "the encapsulant material and the degating region material are chosen such that the adhesive force between the encapsulant material and the degating region material is less than the adhesive force between the encapsulant material and the substrate" as recited in Claim 1, as amended.

In addition, since Mullen, III et al. in view of Erdos does not teach or suggest "a degating region" as recited in Claim 1, as amended, Mullen, III et al. in view of Erdos does not teach or suggest that "the adhesive force between the encapsulant material and the degating region material is less than one half the adhesive force between the encapsulant material and the substrate" as recited in Claim 2, as amended. For this additional reason, Claim 2 is allowable over Mullen, III et al. in view of Erdos.

Further, since Mullen, III et al. in view of Erdos does not teach or suggest "a degating region" as recited in Claim 1, as amended, Mullen, III et al. in view of Erdos does not teach or suggest that "the degating region material is gold" as recited in Claim 4, as amended. For this additional reason, Claim 4 is allowable over Mullen, III et al. in view of Erdos.

For the above reasons, Claim 1 is allowable over Mullen, III et al. in view of Erdos. Claims 2-9, which depend from Claim 1, are allowable for at least the same reasons as Claim 1. Claim 11 is allowable for reasons similar to Claim 1. Claims 12-14, which depend from Claim 11 are allowable for at least the same reasons as Claim 11.

LAW OFFICES OF
SKIJEVEN, MORRILL,
McPHERSON, FRANKLIN
& PHEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-9979

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8. Rejection of Claim 10 under 35 U.S.C. § 103 as being unpatentable over Mullen, III et al. and Erdos as applied to Claims 1-9, and further in view of the Applicant's admitted prior art, Fig. 1.

The Examiner states:

The teachings of modified Mullen are discussed above and it does not disclose the substrate having electrically conductive traces. The applicant's admitted prior art of Fig. 1 discloses a substrate having electrically conductive traces. It would have been obvious to one of ordinary skill in the art at the time of the invention to have made the modified Mullen package with traces so as to provide electrical connections and communications.

As discussed above, Mullen, III et al. in view of Erdos does not teach or suggest "a degating region on the first surface of the substrate" and "a degating region material on the degating region", as recited in Claim 1, as amended. Further, applicant's admitted prior art of Fig. 1 does not teach or suggest "a degating region on the first surface of the substrate" and "a degating region material on the degating region", as recited in Claim 1, as amended.

For the above reason Claim 1 is allowable over Mullen, III et al. and Erdos as applied to Claims 1-9, and further in view of the Applicant's admitted prior art, Fig. 1. Claim 10, which depends from Claim 1, is allowable for at least the same reasons as Claim 1.

9. Gupta, Millerick et al, Kobayashi et al., and Wong considered pertinent by the Examiner to the Applicant's disclosure.

The Examiner states:

Gupta and Millerick et al. disclose degating. Kobayashi et al. and Wong disclose IC packages having solder bump connections.

It is noted that, at a minimum, none of the cited prior art discloses a degating region on the first surface of the substrate and a degating region material on the degating region.

LAW OFFICES OF
SKJRVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

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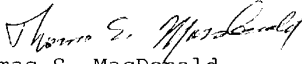
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CONCLUSION

Claims 1-14 and new Claims 23-25 remain in this application. Claims 15-22 have been canceled. For the above reasons, pending Claim 1 is allowable. Claims 2-10 and 23-25, which depend from Claim 1, are allowable for at least the same reasons as Claim 1. Claim 11 is allowable for reasons similar to Claim 1. Claims 12-14, which depend from Claim 11, are allowable for reasons similar to Claim 11. If the Examiner deems a telephone interview helpful to facilitate early allowance of these claims, the Examiner is invited to call the undersigned Attorney for Applicants at (408) 453-9200.

Respectfully submitted,


Thomas S. MacDonald
Attorney for Applicants
Reg. No. 17,774

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on July 12, 1996.

July 12, 1996
Date of Signature


Attorney for Applicants

LAW OFFICES OF
NGJRVEN, MORRILL,
MACPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

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